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Work aimed at extending the maximum frequency capability of CMOS technology, described in Chapters 5 and ... which provides a tunable linear resistive element for integrated circuit filter realisation ...

Chapter 8: Gallium Arsenide Analogue Integrated Circuit Design Techniques
Finishing up on the topic of CMOS bus logic I am going to show a ... Switching gears I am going to talk a bit about the physical layout of integrated circuits.
Shown is an old wafer I have ...

How CMOS Works: Some Final Words

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About CMOSolution

A top-down guide to the design of digital integrated circuits. Reflects industry design methods, moving from VLSI architecture design to CMOS fabrication. Practical hints and tips, case studies, and ...

Digital Integrated Circuit Design from
VLSI Architectures to CMOS
Fabrication

In this paper, a novel approach for very stable physical unclonable function (PUF) is presented based on randomly generated via-hole formation using standard CMOS ... integrated circuits. To guarantee ...

VIA PUF: Ultimately Stable PUF
Design using Random Via Formation
in Standard CMOS Technology
The Belgian research institute expects

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a prototype in standard 28-nm technology to be ready by the end of 2018. At the recent International Microwave Symposium in Philadelphia, Imec announced ...

Imec Demonstrates 140-GHz CMOS Radar-on-Chip with Integrated Antennas

Wireless chipset / SoC design choices are driven by many orthogonal ... is moved to the RF chip and eventually enables an integrated single chip solution. The integration benefits of CMOS The key to ...

System on Chip (SoC) for Short Range Wireless - CMOS versus SiGe

This structure also lets the company design membranes that are either flat or curved. The microphone chip measures 2.5 mm² and the

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diaphragm-has a 1-mm diameter. The company says its CMOS MEMS ...

Hear this: CMOS microphones on a chip
of six-transistor SRAM-bit cells with an area less than 0.25 square microns—half the size of earlier solutions—using conventional bulk CMOS technology and 45nm design rules. Crolles 2 is the ...

Alliance Produces Ultra-Dense SRAM Cell In 45nm CMOS Technology
reduce design space and complexity. Omnivision also features advanced High Dynamic Range (HDR), which helps ensure high-quality image production in various lighting conditions for numerous ...

3 New Image Signal Processors

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Dual work function metal gates are integrated at 17nm spacing between n- and pFETs, highlighting the key benefit of forksheet devices for advanced CMOS area scaling ...
Alternatively, with a forksheet ...

Imec demoes integrated forksheet FETs for 2nm processes
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CMOS High-speed Cameras Market Size 2021 by Consumption, Volume, Average Price, Revenue, Market Share and Trend to 2028

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One technology used in the industry to mitigate this tradeoff is fully depleted silicon-on-insulator (FD-SOI) technology which can operate at 75% lower power as compared to a bulk CMOS process ... We ...

Lattice Leverages FD-SOI for New Low Power FPGAs

With our third generation Keystone DSP design, and the power advantages of 5nm CMOS technology, we are directly addressing our customers' critical needs for low power, highly integrated, high ...

MaxLinear Showcases Industry's First 5nm CMOS 800G PAM4 DSP on TSMC Advanced Process at OFC 2021

Intevac, Inc. (Nasdaq: IVAC) announced today that it has received

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two additional Phase 1 development program awards in Photonics. These awards are ...

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