Hs Can Transceiver With Integrated Galvanic Isolation

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Controller Area

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GM Class 2 Network

Diagnosis Tips

diagnosing CAN communication problem on Volvo S70 Improving my electric longboard with a CAN Bus! What can the CAN Bus do? EB#44 How to read the Can Bus in any car. Quick CAN BUS Check (aka Fun With Resistors) - Wrenchin' Up Using the MAX13054A CAN

Transceiver with High Protection and Multi-Function Standby

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HS-CAN transceiver with integrated galvanic isolation. The TJF1052i

high-speed controller area network (HS-CAN) transceiver provides a galvanically isolated interface between a CAN protocol controller and the physical two-wire HS-CAN bus. It is specifically aimed at industrial applications, where galvanic isolation is necessary to bridge CAN communication between different

voltage domains.

HS-CAN transceiver with integrated galvanic isolation

HS-CAN transceiver with integrated galvanic isolation. Key features. ` 5 kV (RMS) rated isolation voltage, compliant with UL1577, IEC61010 and IEC60950 ` Suitable for 12 V and 24 V systems;

compatible with 3 V to 5 V microcontrollers ` Low electromagnetic emission (EME) and high EMI ` Supports ISO6469 ‘Electrically propelled road vehicles.

HS-CAN transceiver with integrated galvanic isolation

The HS CAN-transceiver family TLE6250 (TLE6250G

and TLE6250GV33) are monolithic integrated circuits that are available as bare die as well as in a PG-DSO-8 package. The ICs are optimized for high speed differential mode data transmission in automotive and industrial applications and they are compatible to ISO/DIS 11898.

Hs Can Transceiver With Integrated Galvanic Isolation

HS-CAN transceiver with integrated galvanic isolation CAN Transceivers Our broad CAN and CAN FD portfolios cover all CAN functions and power modes with high EMC performance, great quality, and a multi-sourced industrial

base. Disruptive innovation in this area opens the door to larger, more flexible and more secure automotive networks in the

Hs Can Transceiver With Integrated Galvanic Isolation

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for a variety of applications. CAN Transceivers - Maxim Integrated Overview. The UJA1161ATK is a ‘self-supplied’ high-speed CAN transceiver with Standby mode integrating an ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant HS-CAN transceiver

Hs Can Transceiver With Integrated Galvanic Isolation

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TLE6250G - Infineon Technologies

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Hs Can Transceiver With Integrated Galvanic Isolation

CAN transceivers interface between the CAN protocol controller and the physical wires of the CAN bus lines.

Our high-speed and low-speed controller area network transceivers offer, integrated isolation, high ESD and high fault protection with value-added features specified by the ISO 11898 standard. Our CAN ICs have integrated protection for more robust communication and handle the CAN bus

connection with high ESD protection for a variety of applications.

CAN Transceivers - Maxim Integrated

Abstract: This application note solves a very common problem of powering an automotive electronic control unit (ECU) with only a 3.3V supply. The ISO 11898-2 standard

stipulates that only a 5V power supply rail powers the CAN transceiver. This article shows how an automotive CAN transceiver can be supplied with a 3.3V charge pump to provide a low power, low-voltage, and easy solution to this ...

Achieve ISO

11898-2-Compliant 5V HS-CAN C - Maxim Integrated

The TLE8250G is a High Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential network which allows data transmission rates up to 1 MBit/s.

Characteristic for a HS CAN network are the two sign al states on the CAN bus: “Dominant”

TLE8250G High Speed CAN-Transceiver

Overview Decription

The TLE9252V is a transceiver designed for HS CAN networks up to 5 Mbit/s in automotive and industrial applications. As an

interface between the physical bus layer and the CAN protocol controller, the TLE9252V drives the signals to the bus and protects the microcontroller against interferences generated within the network.

Product Name - Farnell

The optoCAN-HS system can be used for

the bidirectional optical transmission of CAN-signals with transmission rates of up to 1Mbit/s. It consists of two identical battery supplied transceivers connected to each other with an optical fiber. With the optical transmission and the shielded case, the system is well equipped for EMI and EME tests.

optoCAN-HS

To support these applications the TLE 7263E covers smart po wer functions such as HS- CAN transceiver and LIN transceiver for data transmission, dual low dropout voltage regulator (LDO) for external 5 V supply, and high-side switch as well as a 16-bit SPI (serial

peripheral interface) to control and monitor the IC.

TLE7263 DS 171

Merely said, the hs can transceiver with integrated galvanic isolation is universally compatible similar to any devices to read. Automotive Ethernet-Kirsten Matheus 2014-11-27 Learn how

automotive Ethernet is revolutionizing in-car networking from the experts at the core of its development.

Learn how automotive Ethernet is revolutionizing in-car networking from the experts at the core of its development. Providing

an in-depth account of automotive Ethernet, from its background and development, to its future prospects, this book is ideal for industry professionals and academics alike.

This book addresses the various challenges and open questions relating to CAN communication networks. Opening with

a short introduction into the fundamentals of CAN, the book then examines the problems and solutions for the physical layout of networks, including EMC issues and topology layout. Additionally, a discussion of quality issues with a particular focus on test techniques is presented. Each

chapter features a collection of illuminating insights and detailed technical information supplied by a selection of internationally-regarded experts from industry and academia. Features: presents thorough coverage of architectures, implementations and application of CAN

transceiver, data link layer and so-called higher layer software; explains CAN EMC characteristics and countermeasures, as well as how to design CAN networks; demonstrates how to practically apply and test CAN systems; includes examples of real networks from diverse applications in

automotive engineering, avionics, and home heating technology.

This book introduces a new approach to model and predict substrate parasitic failures in integrated circuits with standard circuit design tools. The injection of majority and minority carriers in the substrate is a recurring problem in

smart power ICs containing high voltage, high current switching devices besides sensitive control, protection and signal processing circuits. The injection of parasitic charges leads to the activation of substrate bipolar transistors. This book explores how these events can be evaluated for a wide range of

circuit topologies. To this purpose, new generalized devices implemented in Verilog-A are used to model the substrate with standard circuit simulators. This approach was able to predict for the first time the activation of a latch-up in real circuits through post-layout SPICE simulation analysis. Discusses

substrate modeling and circuit-level simulation of parasitic bipolar device coupling effects in integrated circuits; Includes circuit back-annotation of the parasitic lateral n-p-n and vertical p-n-p bipolar transistors in the substrate; Uses Spice for simulation and characterization of parasitic bipolar

transistors, latch-up of the parasitic p-n-p-n structure, and electrostatic discharge (ESD) protection devices; Offers design guidelines to reduce couplings by adding specific protections.

This book is a step-by-step tutorial on how to design a low-power, high-resolution (not less

than 12 bit), and high-speed (not less than 200 MSps) integrated CMOS analog-to-digital (AD) converter, to respond to the challenge from the rapid growth of IoT. The discussion includes design techniques on both the system level and the circuit block level. In the architecture level, the power-efficient

pipelined AD converter, the hybrid AD converter and the time-interleaved AD converter are described. In the circuit block level, the reference voltage buffer, the opamp, the comparator, and the calibration are presented. Readers designing low-power and high-performance AD converters won’t

want to miss this invaluable reference. Provides an in-depth introduction to the newest design techniques for the power-efficient, high-resolution (not less than 12 bit), and high-speed (not less than 200 MSps) AD converter; Presents three types of power-efficient architectures of the high-

resolution and high-speed AD converter; Discusses the relevant circuit blocks (i.e., the reference voltage buffer, the opamp, and the comparator) in two aspects, relaxing the requirements and improving the performance.

This book explores the unique advantages and

large inherent transmission capacity of optical fiber communication systems. The long-term and high-risk research challenges of optical transceivers are analyzed with a view to sustaining the seemingly insatiable demand for bandwidth. A broad coverage of topics relating to the design of high-speed

optical devices and integrated circuits, oriented to low power, low cost, and small area, is discussed. Written by specialists with many years of research and engineering experience in the field of optical fiber communication, this book is essential for an audience dedicated to the development of integrated electronic

systems for optical communication applications. It can also be used as a supplementary text for graduate courses on optical transceiver IC design. Contents: Design Considerations for Integrated Modulator Drivers in Silicon Germanium Technology (S Pavan et al.); Compact Low-

Noise Pulse Generating Lasers with Repetition Rates of 10 to 50 GHz (G Spuehler et al.); Integrated Wide-Band CMOS Duobinary Transmitter for Optical Communication Systems (R Tao & M Berroth); A 10 Gb/s Equalizer with Integrated Clock and Data Recovery for Optical Communication

Systems (D S McPherson et al.); Equalizer Architectures for 40-Gb/s Optical Systems Limited by Polarization-Mode Dispersion (J Sewter & A C Carusone); Trade-offs in High-Speed Serial Link ICs (S Li); High-speed Architectures and Building Blocks for Clock and Data

Recovery Systems (C S Vaucher et al.); MOS Current Mode Logic Circuits: Design Considerations in High-Speed Low-Power Applications and Future Trends, a Tutorial (Y Liu et al.); Recent Progress in 40- to 100-Gbit/s-Class Optical Communications ICs Using InP-Based HBT

Technologies (K Ishii et al.); 40 Gb/s TDM System Transceiver Prototype in InP HBT Technology (K Krishnamurthy et al.); Enhanced Network Signaling for 10 Gigabit Ethernet to Achieve a LAN-WAN Seamless Interface and Its Implementation in the PHY-LSI/Transceiver Module (H Ichino et

al.). Key Features Wide range of topics relating to the design of high-speed optical transceivers Analysis of the long-term risks and hard-going research challenges of optical transceivers from professionals Useful for readers dedicated to the development of integrated electronic systems for optical

communication applications Readership: Engineers, researchers, practitioners, academics, upper level and undergraduates in integrated circuits and device design in the fields of electronic engineering, semiconductor physics and microelectronics.

"This book presents a

unique integration of knowledge from multidisciplinary fields of engineering, industrial design, and medical science for the healthcare of a specific user group"--Provided by publisher.

This book investigates and discusses the hardware design and implementation to

achieve smart air interfaces with a reduced number of Radio Frequency (RF) transmitter and receiver chains, or even with a single reconfigurable RF-Frontend in the user terminal. Various hardware challenges are identified and addressed to enable the implementation of autonomous

reconfigurable RF-Frontend architectures. Such challenges are (i) the conception of a transceiver with wide tuning range of at least up to 6 GHz, (ii) the system integration of reconfigurable technologies targeting current compact devices that demand voltages up to 100 V for adaptive controlling and (iii) the

realization of a multiband and multistandard antenna module employing agile components to provide flexible frequency coverage. A solid design of a reconfigurable frontend is proposed from the RF part to the digital baseband. The system integration of different components in the reconfigurable RF-

Frontend of a portable-oriented device architecture is demonstrated.

Providing a comprehensive insight into today's standard technologies, this book covers the vast range of semiconductor products and their possible applications. The material ranges from the

basics of conventional semiconductor technology through standard, power and opto semiconductors, to highly complex memories and microcontrollers and the special devices and modules for smartcards, automotive electronics, consumer electronics and telecommunications.

Several chapters are devoted to the production of semiconductor components and their use in electronic systems, as well as to quality management. The book offers both students and users a unique overview of technology, architecture and areas of application of semiconductor

products. The enclosed CD-ROM includes data on a multitude of products.

The work establishes the design flow for the optimization of linear CMOS power amplifiers from the first steps of the design to the final IC implementation and tests. The authors also focuses on design

guidelines of the inductor's geometrical characteristics for power applications and covers their measurement and characterization. Additionally, a model is proposed which would facilitate designs in terms of transistor sizing, required inductor quality factors or minimum supply voltage. The model

considers limitations that CMOS processes can impose on implementation. The book also provides different techniques and architectures that allow for optimization.

"Today, high-speed integrated circuits (ICs) are advancing rapidly, driven by the ever-increasing demands for

larger bandwidth and better energy efficiency in high performance computing and communications. This is evident in several research areas involving the most critical components in these applications such as on-chip clocking and interconnect. In addition, high-speed ICs are enabling emerging

sensing applications, for Internet of Things such as short-distance radars. In recent years, high-speed ICs have gradually migrated from III-V technologies to silicon-based technologies, driven by the latter's rapid advances in device performance, significant cost advantage, and system-on-a-chip (SoC)

capability. However, designing silicon-based high-speed ICs still faces many challenges, such as significant parasitics effects and large signal attenuation due to the lossy silicon substrate. Moreover, high energy efficiency becomes increasingly important, especially in mobile and densely populated devices. In

this thesis, I will address these challenges in three different high-speed circuits and systems targeting emerging computing and sensing applications, namely, a) injection-locking frequency multiplier (ILFM), b) a new on-chip transmission-line based interconnect system, and c) an integrated light

detection and ranging (LIDAR) system. Recently, the injection locking circuit technique is increasingly used in high-speed clock generation and distribution, thanks to its advantages in high operation frequency and low power consumption. In this work, a new ILFM is proposed and

designed for on-chip clock distribution applications. It uses multiphase injection and built-in harmonic generation to increase locking range and reduce power consumption. Two multiply-by-2 ILFM prototypes are implemented in 130-nm CMOS technology, and achieve wide locking

range up to 116%, low power consumption, and compact chip area. The global interconnects for data communications in a multi-core chip become increasingly critical. Compared to the network-on-chip approach, the proposed transmissionline based interconnect system exhibits significant advantages in

bandwidth, circuit complexity, latency, and energy efficiency. As part of a collaborative project, energy-efficient high-speed circuits are designed for this interconnect system. The prototype is implemented in 130-nm BiCMOS technology, and achieves date rates up to 25.4 Gb/s with energy efficiency 1.67

pJ/b. LIDARs are increasingly adopted in smart sensor systems. In this work, a LIDAR system is proposed for emerging medical sensing applications. Based on the pulsed time-of-flight principle, the LIDAR system integrates an optical transceiver and optical devices. My work focuses on energy-

efficient high-speed LIDAR transceiver design. The fully integrated transceiver prototype is designed in 130-nm BiCMOS technology, and has a measurement range of 0.5-10 m, an accuracy less than 130 ps, and a power consumption of 39.5 mW. In summary, by new circuit techniques and careful

design, silicon-based ICs can achieve high-speed and good energy efficiency for emerging computing and sensing applications."--Pages iv-v.